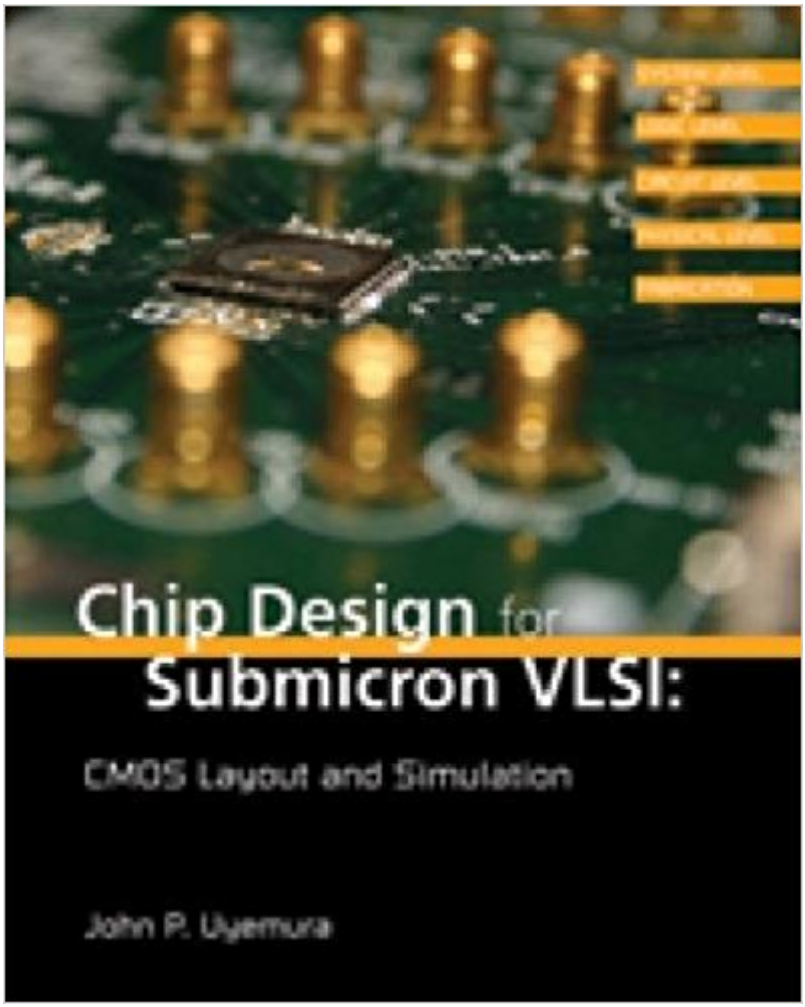
Chip Design For Submicron VLSI: CMOS Layout And Simulation



Synopsis

The text is organized around first introducing the global view of digital integrated circuit design, VLSI and design automation, and then sequentially developing the topics from the materials and devices level, up through the circuits and then system level. This mirrors the structural hierarchy of the chip design field itself. While building a solid foundation and reference for the chip design, it integrates the discussion with hands-on examples of the design automation software, included in the book, to illustrate not only the layout and simulation concepts, but also how an industry designer would put them into practice. Both theory and application are effectively integrated into a cohesive treatment of the subject and art of chip design.

Book Information

Hardcover: 432 pages

Publisher: CL Engineering; 1 edition (February 8, 2005)

Language: English

ISBN-10: 053446629X

ISBN-13: 978-0534466299

Product Dimensions: 8.1 x 0.8 x 9.5 inches

Shipping Weight: 2 pounds (View shipping rates and policies)

Average Customer Review: 5.0 out of 5 stars 2 customer reviews

Best Sellers Rank: #693,440 in Books (See Top 100 in Books) #30 inÃ Â Books > Engineering & Transportation > Engineering > Electrical & Electronics > Circuits > VLSI & ULSI #216 inÃ Â Books > Engineering & Transportation > Engineering > Electrical & Electronics > Circuits > Design #380 inÃ Â Books > Engineering & Transportation > Engineering > Civil & Environmental > Structural

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Chapter 1. Installing the Microwind Software 1.1 Getting Started 1.2 Exploring Microwind 1.3 Installing Dsch 1.4 Plan of the Book 1.5 Some Important Details 1.6 References Chapter 2. Views of a Chip 2.1 The Design Hierarchy 2.2 Integrated Circuit Layers 2.3 Photolithography and Patter Transfer 2.4 Planarization 2.5 Electrical Characteristics 2.6 Silicon Characteristics 2.7 Overview of Layout Design 2.8 References 2.9 Exercises Chapter 3. CMOS Technology 3.1 Meet the MOSFETs 3.2 CMOS Fabrication 3.3 Submicron CMOS Processes 3.4 Process Technologies in Microwind 3.5 Masks and Layout 3.6 The Microwind MOS Generator 3.7 Chapter Summary and Roadmap 3.8 References 3.9 Exercises Chapter 4. Using a Layout Editor 4.1 Lambda-Based Layout 4.2

Rectangles and Polygons 4.3 The MOS Generator Revisited 4.4 Summary 4.5 Exercises Chapter 5. CMOS Design Rules 5.1 Types of Rules 5.2 The SCMOS Design Rule Set 5.3 FET Layout 5.4 References 5.5 Exercises Chapter 6. MOSFETs 6.1 MOSFET Operation 6.2 MOSFET Switch Models 6.3 The Square Law Model 6.4 MOSFET Parasitics 6.5 Comments on Devise Layout 6.6 References 6.7 Exercises Chapter 7. MOSFET Modeling with SPICE 7.1 SPICE Levels 7.2 MOSFET Modeling in Microwind 7.3 Circuit Extraction 7.4 Microwind Level 3 and BSIM4 Equations 7.5 References 7.6 Exercises Chapter 8. CMOS Logic Gates 8.1 The Inverter 8.2 NAND and NOR Gates 8.3 Complex Logic Gates 8.4 The Microwind Compile Command 8.5 Tri-State Circuits 8.6 Large FETs 8.7 Transmission Gates and Pass Logic 8.8 References 8.9 Exercises Chapter 9. Standard Cell Design 9.1 Cell Hierarchies 9.2 Cell Libraries 9.3 Library Entries 9.4 Cell Shapes and Floor Planning 9.5 References 9.6 Exercises Chapter 10. Storage Elements 10.1 SR Latch 10.2 Bit-level Register 10.3 D-type Flip Flop 10.4 Dynamic DFF 10.5 The Static RAM Cell 10.6 References 10.7 Exercises Chapter 11. Dynamic Logic Circuits 11.1 Basic Dynamic Logic Gates 11.2 Domino Logic 11.3 Self-Resetting Logic 11.4 Dynamic Memories 11.5 References 11.6 Exercises Chapter 12. Interconnects 12.1 Modeling an Isolated Line 12.2 Long Interconnects 12.3 Crosstalk Capacitances 12.4 Interconnect Wiring Tools 12.5 General Routing Techniques 12.6 References 12.7 Exercises Chapter 13. System Layout 13.1 Power Supply Distribution 13.2 Pad Generation 13.3 Input and Output Circuits 13.4 The Logo Generator 13.5 References 13.6 Exercises Chapter 14. SOI Technology 14.1 Modern SOI CMOS 14.2 Why SOI? 14.3 Problems with SOI 14.4 SOI in Microwind 14.5 References 14.6 Exercises Chapter 15. Digital System Design 1 15.1 A First Look 15.2 Editing Features 15.3 Creating a Logic Schematic 15.4 Simulating a Logic Design 15.5 Creating a Macro Symbol 15.6 Creating A Verilog (R) Listing 15.7 The DSCH-Microwind Design Flow 15.8 Using a Design Toolset 15.9 MOSFETs in Dsch 15.10 References 15.11 Exercises Chapter 16. Digital System Design 2 16.1 A 4-bit Binary Adder 16.2 Carry Lookahead Adder 16.3 Pipeline Register 16.4 Divide-by-N Circuit 16.5 Binary Counter 16.6 Summary 16.7 References 16.8 Exercises Chapter 17. Capacitors and Inductors 17.1 Integrated Capacitors 17.2 Integrated Inductors 17.3 References 17.4 Exercises Chapter 18. Analog CMOS Circuits 18.1 Simple Amplifiers 18.2 MOSFETs 18.3 Resistors 18.4 Signal Wiring 18.5 Summary 18.6 References 18.7 Exercises Appendix 1. Microwind Command Summary A.1 File A.2 View A.3 Edit A.4 Simulate A.5 Compile A.6 Analysis A.7 Help A.8 Menu Bar A.9 Other Screens Appendix 2. Microwind CMOS Technology Files Index

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Technology.

The "Chip Design for Submicron VLSI" written by John Uyemura was like brand new, even though I was buying it as a used book from . My experience with was always very good. They are very prompt in delivering the items in time. Many many thanks for the good work. I am very happy to recommend to anyone.

I would like to write about "Chip Design for Submicron VLSI:CMOS Layout and Simulation" book (2006 ed.,THOMSON), written by John P. Uyemura.General : As the author mentioned that the book is a basic introduction to submicron CMOS designs,you will find the book contents organized into short chapterswith a level of details that one can study and understand within a short period.The software(Microwind and Dsch) that comes with the book is a nice tool to start learning CMOS VLSI layout and simulation.It would be best to practice asyou read and understand each section or topic.You can learn much from hands on by doing your own version of layouts or circuits for simulation.Each figure of a layout shown in the book is usually large enough to clearly see the details.Thus, you can try to recreate your own layout as seen fromthe figure.An important note about using Dsch program should be given here.In a Dsch schematic,you cannot name an input with "/" as a part of the name,if you planto compile the circuit to Verilog code,otherwise you will get a Compile Verilog file error.Author’s Writing Style: The author is one of well known writers in the field of CMOS VLSI circuits and systems.If you have seen this book,and maybe also some other bookswritten by him in a book store,you probably agree that his books are quite easy to read due to a clear and concise organization and a way he usuallywrites to convey information and present ideas.Key words are usually highlighted in each section.This helps for finding related explanation or specificconcepts and ease of reviews.Errata: I found only a few(might be sent to publisher), the book is well written.The information here about the content should help anyone who feel interested to have some ideas about how much the book is directly useful for his or her application or learning interest.Contents: 406 pages of content,a small book. Each chapter contains a short list of References and a few excercise problems at the end of each chapter.- Chapter 1 Installing the Microwind Software (15 pages)- Chapter 2 Views of a Chip--Layers and Patterns (21 pages)- Chapter 3 CMOS Technology--A Basis for Design(27 pages)- Chapter 4 Using a Layout Editor--Fundamental Concepts (18 pages)- Chapter 5 CMOS Design Rules--Guidelines for Layout (23 pages)- Chapter 6 MOSFETs--Operation and Analytical Models (26 pages)- Chapter 7 MOSFET Modeling with SPICE (23 pages)- Chapter 8 CMOS Logic Gates--Design and Layout (41 pages)-

Chapter 9 Standard Cell Design--Layouts and Wiring (22 pages)- Chapter 10 Storage Elements--Design and Layout (15 pages) - Chapter 11 Dynamic Logic Circuits--Basic Principles (14 pages)- Chapter 12 Interconnect--Routing and Modeling (20 pages)- Chapter 13 System Layout--Physical Design of the Chip (23 pages)- Chapter 14 SOI Technology--Introduction to Basics (12 pages)- Chapter 15 Digital System Design 1--The Dsch Program (28 pages)- Chapter 16 Digital System Design 2--Design Flow Examples (22 pages)- Chapter 17 Capacitors and Inductors On-Chip Passive Elements (12 pages)- Chapter 18 Analog CMOS Circuits Layout Basics (17 pages) - Appendix A Microwind Command Summary (8 pages) The appendix contains a summary of the Menu options in Microwind,each pointed with an arrow and short description. A.1 File- the group of commands for all file operations; A.2 View- commands to control the appearance of layout drawing; A.3 Edit- commands to do basic object manipulations and custom placement of rectangles; A.4 Simulate- commands for SPICE simulations,2D and 3D viewers; A.5 Compile- two commands for automated design; A.6 Analysis- DRC,Measurement tool and Parametric Analysis(some versions); A.7 Help- access to online versions of design rules and reference manual; A.8 Menu Bar- shortcut buttons formajor operations,both left-side buttons and right-side buttons shown; A.9 Other Screens- refer to the online Help function and User's Manual.- Appendix B Microwind CMOS Technology Files (11 pages) Explanation about parameter listing and parameters defined in .rul files.The sample listing is from the cmos018.rul file.The values contained in the file are,for example,layer information,design rules,device parameters,parasitics,CIF layer definitions,data for 2D and 3D views.----Sittinart N.

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